

Publication Details

The paper which this data accompanies has been submitted for a presentation at this conference: IEEE International Conference on Microelectronic Test Structures 2016, which will take place in Yokohama, Japan in March 28-31 2016.

Chip level characterisation studies of Ni and NiFe electrochemical deposition using test structures

J. Murray, R. Perry, J.G. Terry, S. Smith, A.R. Mount, A.J. Walton

Abstract — This paper describes the first use of test structure chips designed to characterise the fundamental properties of Ni and NiFe alloy films deposited using electroplating. This approach is used to perform a chip-level investigation into the effects of electrolyte bath composition on the characteristics of deposited Ni and NiFe layers. The advantage of this methodology is that each electrolyte change does not require the replacement of a 35 litre bath (which is necessary for wafer level investigations), thereby making each experiment far less time consuming, and considerably cheaper to perform.